CLAIMS

1. An automotive computing device memory system comprising:

non-volatile storage configured to hold object store pages for an automotive computing device;

dynamic random access memory (DRAM) operably associated with the non-volatile storage and configured to receive object store pages; and

static random access memory (SRAM) operably associated with the non-volatile memory and configured for connection to a battery so that one or more object store pages can be preserved therein in the event of an automotive power loss.

2. The automotive computing device memory system of claim 1, wherein the non-volatile storage comprises flash memory.

3. The automotive computing device memory system of claim 1, wherein the DRAM comprises one or more DRAMs or SDRAMs.

4. The automotive computing device memory system of claim 1 further comprising a battery operably couplable with the SRAM responsive to an automotive power loss.

5. The automotive computing device memory system of claim 4 further comprising means for operably coupling the battery with the SRAM in the event of an automotive power loss.

6. The automotive computing device memory system of claim 4, wherein the battery comprises a single cell battery.

7. The automotive computing device memory system of claim 4, wherein the battery comprises a lithium cell battery.

8. An automobile embodying the memory system of claim 1.

9. An automotive computing device memory system comprising:

non-volatile storage means configured to hold object store pages for an automotive computing device;

dynamic random access memory (DRAM) means operably associated with the non-volatile storage means and configured to receive object store pages;

static random access memory (SRAM) means operably associated with the non-volatile memory and configured for connection to a battery so that one or more object pages can be preserved therein in the event of an automotive power loss;

battery means for providing backup power to the SRAM; and

circuit means for detecting a power loss and responsive thereto operably coupling the battery with the SRAM in the event of an automotive power loss.

10. An automotive computing device comprising:

one or more microprocessors configured to be powered by a automotive voltage source;

static random access memory (SRAM) operably coupled with the one or more microprocessors, the SRAM being configured to receive one or more pages, under the influence of the one or more microprocessors, from one or more of non-volatile storage or volatile storage that can be carried by an automotive vehicle; and

a backup battery couplable with the SRAM to provide power in the event that the automotive voltage source drops out of regulation.

11. The automotive computing device of claim 10 further comprising power control circuitry associated with the SRAM and configured to determine when the automotive voltage source drops out of regulation and then automatically couple the backup battery with the SRAM.

12. The automotive computing device of claim 11, wherein the power control circuitry is configured to place the SRAM in a low power, high impedance state.

13. The automotive computing device of claim 11, wherein the power control circuitry is configured to isolate the SRAM and the backup battery from other system components.

14. The automotive computing device of claim 11, wherein the power control circuitry is configured to place the SRAM in a low power, high impedance state, and then subsequently couple the SRAM with the backup battery.

15. The automotive computing device of claim 10 further comprising non-volatile storage operably coupled with the one or more microprocessors and configured to contain an object store for the computing device.

16. The automotive computing device of claim 15, wherein the non-volatile storage comprises flash memory.

17. The automotive computing device of claim 15, wherein the volatile storage from which the SRAM is configured to receive the one or more pages comprises DRAM configured to hold read only pages from the object store.

18. The automotive computing device of claim 15, wherein the volatile storage from which the SRAM is configured to receive the one or more pages comprises DRAM configured to only hold read only pages from the object store.

19. The automotive computing device of claim 15, wherein the SRAM is configured to hold pages that have been written to.

20. The automotive computing device of claim 19, wherein the SRAM is configured to hold at least some read only pages that are written to.

21. The automotive computing device of claim 10 further comprising low voltage detection circuitry operably coupled with the one or more microprocessors and configured to detect when the automotive voltage source has dropped out of regulation and generate a signal to the microprocessor indicating the same.

22. The automotive computing device of claim 21, wherein the one or more microprocessors are configured to receive said signal and effect one or more copy operations responsive thereto.

23. The automotive computing device of claim 22, wherein said copy operations can copy pages from volatile storage to SRAM.

24. An automobile embodying the automotive computing device of claim 10.

25. An automotive computing device comprising:

one or more SRAMs;

one or more backup batteries; and

power control circuitry configured to:

detect when a voltage powering the one or more SRAMs has dropped out of regulation; and

automatically incorporate the one or more backup batteries to power the one or more SRAMs.

26. The automotive computing device of claim 25, wherein the one or more backup batteries comprise one or more cell batteries.

27. The automotive computing device of claim 25, wherein the one or more backup batteries comprise one or more lithium cell batteries.

28. The automotive computing device of claim 25, wherein the power control circuitry is configured to place the one or more SRAMs in a low power state.

29. The automotive computing device of claim 25, wherein the power control circuitry is configured to isolate the one or more backup batteries and the one or more SRAMs from other system components.

30. The automotive computing device of claim 25, wherein the power control circuitry is configured to place the one or more SRAMs in a low power state before it incorporates the one or more backup batteries to power the one or more SRAMs.

31. An automobile embodying the computing device of claim 25.

32. An automotive computing system comprising:

one or more backup batteries;

one or more SRAMs selectively couplable to the one or more backup batteries and configured to hold one or more pages that have been written to in the

computing system, the one or more backup batteries being provided so that they can be coupled to the SRAM in an event of an abrupt power shut down.

33. The automotive computing system of claim 32, wherein the one or more backup batteries comprise cell batteries.

34. An automotive computing system comprising:

one or more microprocessors configured to be powered by a vehicle voltage source;

non-volatile storage coupled with the one or more microprocessors and configured to hold one or more object store pages for the computing system;

volatile storage coupled with the one or more microprocessors and configured to hold one or more object store pages that it receives from the non-volatile storage;

static random access memory (SRAM) operably coupled with the one or more microprocessors, the SRAM being configured to receive one or more pages, under the influence of the one or more microprocessors, from one or more of the non-volatile storage or volatile storage;

a backup battery couplable with the SRAM to provide power in the event that a voltage rail associated with the voltage source drops out of regulation;

low voltage detection circuitry operably coupled with the one or more microprocessors and configured to detect when the voltage rail drops below a predetermined value and generate a signal to the one or more microprocessors indicating the same; and

power control circuitry configured to:

detect when the voltage rail drops out of regulation; and

automatically incorporate the backup battery to power the SRAM.

35. A vehicle embodying the computing system of claim 34.

36. An automotive computing device data preservation method comprising:

detecting when a voltage associated with operation of an automotive vehicle drops out of regulation;

responsive to said detecting, placing an SRAM carried on the automotive vehicle in a low power state; and

backing up the SRAM with a backup battery.

37. The automotive computing device data preservation method of claim 36 further comprising placing the SRAM in the lower power state before backing up the SRAM with the backup battery.

38. The automotive computing device data preservation method of claim 36 further comprising isolating the backup battery and the SRAM from other system components.

39. The automotive computing device data preservation method of claim 36 further comprising after said detecting, writing data from DRAM carried on the automotive vehicle into the SRAM.

40. An automotive computing device data preservation method comprising:

detecting an abrupt automotive vehicle power shut down;

responsive to said detecting, placing an SRAM carried on the automotive vehicle in a low power state; and

backing up the SRAM in its low power state with a backup battery.

41. The automotive computing device data preservation method of claim 40 further comprising placing the SRAM in the lower power state before backing up the SRAM with the backup battery.

42. The automotive computing device data preservation method of claim 40 further comprising isolating the backup battery and the SRAM from other system components.

43. An automotive computing device data preservation method comprising:

maintaining an object store for the computing device in flash memory that is carried by an automotive vehicle;

writing pages of the object store into DRAM that is carried by the automotive vehicle;

writing pages of the DRAM into SRAM that is carried by the automotive vehicle in the event the DRAM pages are attempted to be written to; and

battery-backing the SRAM in the event of an abrupt power shut down condition.

44. The automotive computing device data preservation method of claim 43 further comprising detecting the abrupt power shut down condition and responsive thereto, placing the SRAM in a low power state.

45. The automotive computing device data preservation method of claim 44 further comprising placing the SRAM in the lower power state before battery-backing the SRAM.

46. The automotive computing device data preservation method of claim 43 further comprising isolating the battery-backed SRAM from other system components.

47. The automotive computing device data preservation method of claim 43 further comprising copying one or more pages from DRAM to SRAM in the event of the power shut down condition.

48. A method of operating an automotive computing device comprising:

providing an automotive computing device having flash memory that can contain read only pages, DRAM for holding pages from the flash memory, and SRAM for holding DRAM pages that are written to;

detecting when a voltage powering the SRAM drops out of regulation;

placing the SRAM in a low power state responsive to said voltage dropping out of regulation; and

backing up the SRAM with a backup battery.

49. The method of claim 48 further comprising backing up the SRAM with the backup battery after placing the SRAM in the low power state.